Finding Setup/Hold Timing Violation

Analyze And Measure Sequential Logic Timing Statistically

The analysis and location of timing errors in sequential logic circuits goes beyond merely triggering on a timing anomaly. Statistical analysis helps the designer understand the nature and cause of the problem. Trend analysis provides a fast way to locate timing errors in long data records.

Triggering on a single anomaly, such as a setup time violation, can be helpful in studying individual timing events. A setup time sensitive trigger is show in figure 1 A more complete picture of a timing problem is obtained by using histogramming. In figure 2 the clock to data delay parameter, Δc2d -, is histogrammed (Trace A) to see timing errors in over 1,000,000 clock cycles signal. The histogram is displayed with logarithmic vertical scaling where each division represents a 10:1 factor in the number of setup time violations. Errors, indicated by the smaller distribution, occur at a rate of about 1 in 2000 clock cycles.

Trace B is a trend graph of the same parameter. It shows the cycle to cycle variation in setup time over the 10,000 clock cycles represented in each acquisition. Note that there are 2 narrow pulses which mark the location of the timing anomalies.

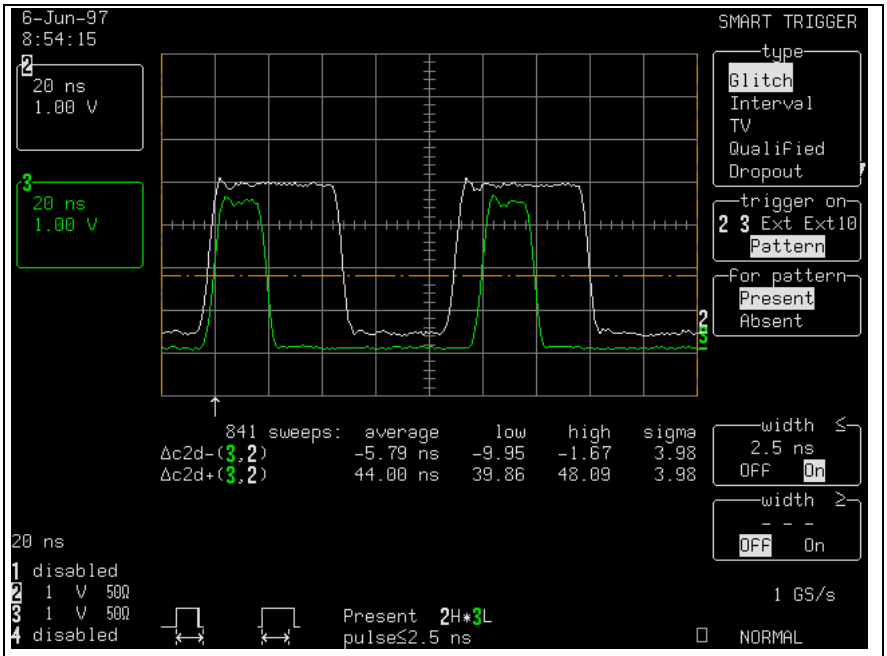

Figure 1 - Setup/hold trigger setup using SMART TRIGGER. The time between the data and clock transitions is measured using a logic pattern glitch trigger.

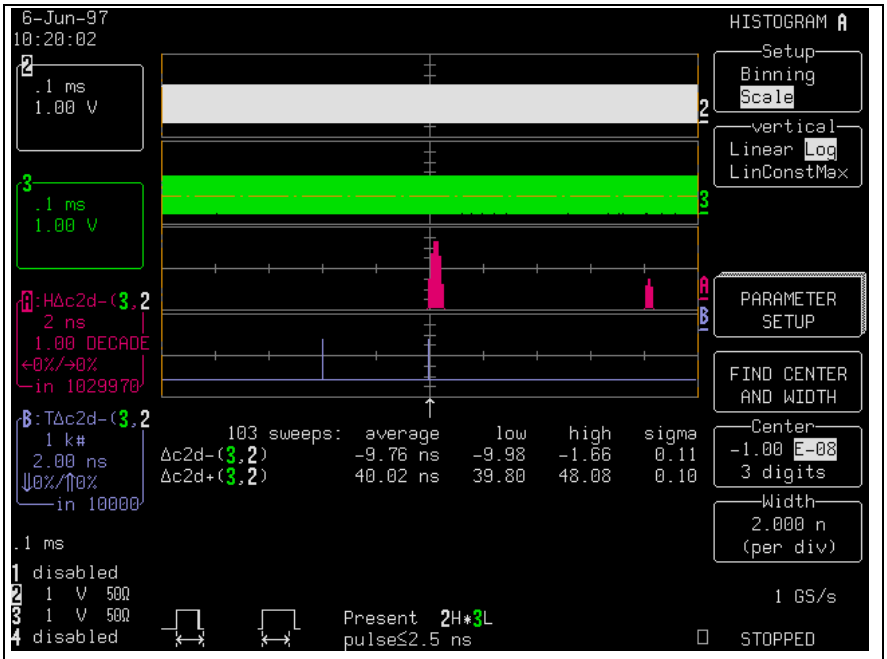

Figure 2 - Histogram of clock to data delay detects timing violation. Trend graph locates violation in acquired waveform

In figure 3 the areas of the acquired waveforms, traces 2 and 3, corresponding to the locations indicated by the trend graph are expanded horizontally using zoom displays. It is easy to see the pulse pair, located at the center of the trace, with a setup time of 1.66 ns.

Note that the timing measurement parameters, such as Δc2d -, have a timing resolution of 10 ps. This means that histogram and trend based analysis provides usable timing information even for the fastest logic families. They are not limited by the minimum timing resolution of the trigger circuits.

In the final example, shown in figure 4, pass fail testing is used to automatically acquire individual timing errors. Testing is based on setup times which are smaller than 3 ns. This particular test has been set to stop the acquisition on failure. It could also have easily been setup to store the waveform or to provide a hard copy of the error using an optional high speed internal printer.

LeCroy Oscilloscopes offer the most complete package of timing analysis tools offering resolution to 10 ps on up to 2,000,000,000 measurements as well as the ability to locate specific events in timing waveform of up to 20,000 cycles.

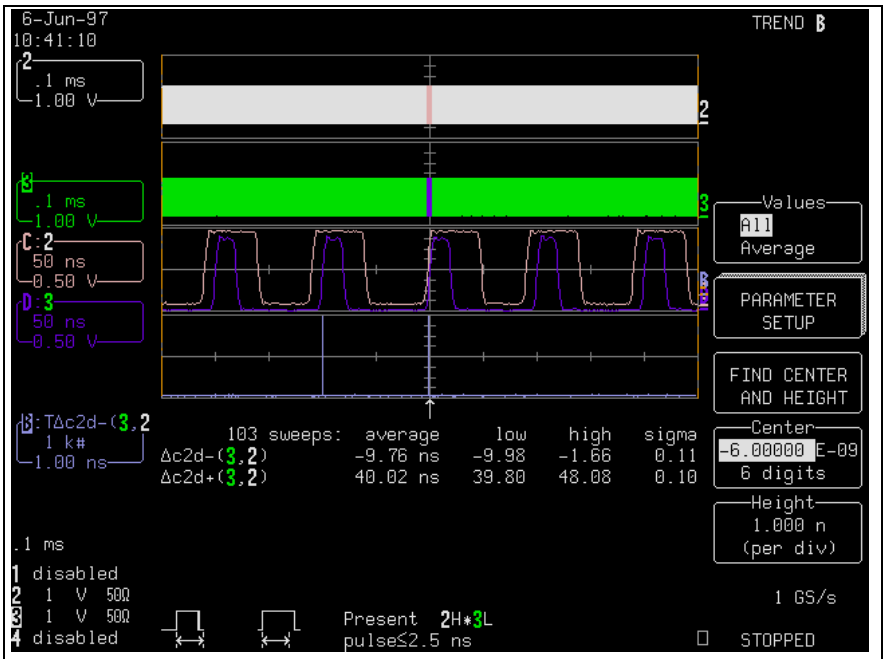

Figure 3 - Trend graph, trace B, points out location of timing violation in a which is viewed using zoom traces C & D.

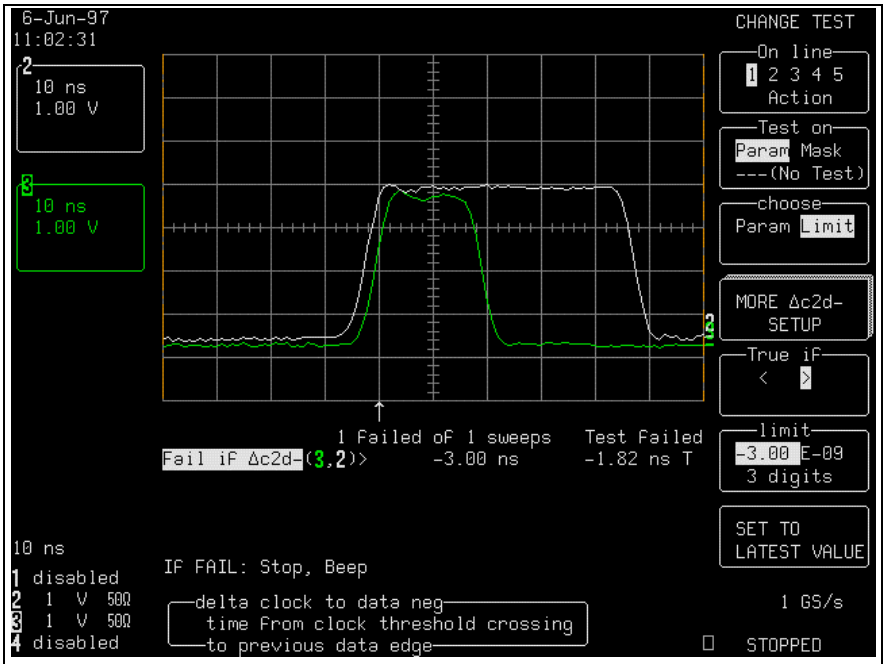

Figure 4 - Using pass/fail testing based on clock to data delay, Δc2d-, captures individual timing events